

Application No. 10/734,763  
Amendment dated August 17, 2007  
Reply to Office Action of April 17, 2007

Docket No.: 20910/0205488-US0

## REMARKS

Claims 1-3, 6-17, 20-22, and 25-36 are pending. By this Amendment, Claims 1, 6, 20, 25, 26 and 31 are amended, and Claims 4, 18 and 23 are canceled. Claims 5, 19 and 24 were previously canceled.

With respect to amended independent Claims 1, 6, 20, 25 and 31, see for example the originally filed specification at numbered paragraph [1028].

Applicant gratefully acknowledges the Examiner's indication that Claims 7, 26, 32 and 36 contain allowable subject matter. (Note that Claim 26 is not rejected under either of §§ 103(a), 102).

**Claim Rejection – 35 U.S.C. §112**

In the Office Action the Examiner rejects Claim 26 under 35 U.S.C. 112. Amended Claim 26 obviates this rejection.

### Claim Rejection – 35 U.S.C. §102

In the Office Action the Examiner rejects Claims 4, 18 and 23 under 35 U.S.C. 102(b) as being anticipated by Prabhu (US Patent No. 6,463,525, hereinafter Prabhu). Cancellation of Claims 4, 18 and 23 obviates this rejection.

### Claim Rejections – 35 U.S.C. §103

In the Office Action the Examiner rejects Claims 1-3, 6, 8-17, 20-22, and 25, 27-31, and 33-35 under 35 U.S.C. 103(a) over Nair (US Patent No. 6,195,746) and Gaertner (US Patent No. 6,237,076) in various combinations with Prabu and Yeager (U.S. Patent No. 6,216,200). These rejections are respectfully traversed.

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The Examiner cites Gaertner at Figure 1 and C3/L31-C4/L16 as teaching replacing a lesser width source specifier in a lesser width consumer instruction with a greater width source specifier.

However, as explained below, the cited section of Gaertner does not disclose or suggest modifying a lesser width consumer instruction, does not disclose or suggest replacing a lesser width consumer instruction's source specifier with a greater width source specifier, and does not disclose or suggest a lesser width consumer instruction executing with a greater width source specifier.

Further, the cited section of Gaertner does not appear to disclose or suggest renaming a 32 bit register to a 64 bit register.

Gaertner at Figure 1 and C3/L31-C4/L16 discloses a 32 bit Instruction No. 2 depending from a 64 bit Instruction No. 1 (e.g. C3/L34). Gaertner further discloses that the 64 bit Instruction No. 1 places bits 00-64 from Physical Register 20 (Logical Register 5) into locations 00-64 of Physical Register 12 (Logical Register 4). Then, the 32 bit Instruction No. 2 copies bits from locations 00-31 of Physical Register 12 (Logical Register 4) into locations 00-31 of Physical Register 13.

There is no mention of a greater width source specifier for the 32 bit Instruction No. 2, much less modification of the Instruction No. 2 by substituting in a different source specifier. If anything, Gaertner appears to suggest renaming a 64 bit register (the Physical Register 12, Logical Register 4) to a 32 bit register (which is the opposite of the Examiner's assertion that Gaertner renames a 32 bit register to a 64 bit register), since the 32 bit Instruction No. 2 simply copies the lower 32 bits of the 64 bit register modified by the 64 bit Instruction No. 1.

Accordingly, Gaertner fails to disclose or suggest *"a processor modifying the lesser width consumer instruction by substituting for execution a greater width source register specifier for a lesser width source register specified in the lesser width consumer instruction"*, as recited in Claim 1, and similar features recited in independent Claims 6, 20, 25 and 31. Nair, Prabu, and

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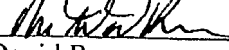
Yeager fail to overcome this deficiency of Gaertner. Accordingly, all the claims are allowable over Gaertner, Nair, Prabu and Yeager.

Withdrawal of the claim rejections under 35 U.S.C. § 103(a) is respectfully requested.

In the event any questions arise regarding this communication or the application in general, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Dated: August 17, 2007

Respectfully submitted,

By   
M. David Ream

Registration No.: 35,333  
DARBY & DARBY P.C.  
P.O. Box 5257  
New York, New York 10150-5257  
(206) 262-8900  
(212) 527-7701 (Fax)  
Attorneys/Agents For Applicant

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